Appl. No. 10/710,023
Amdt. Dated August 1, 2005
Reply to Office Action of 5/10/2005

AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently amended) A multi-layered lithography structure, the structure comprising:
a substrate;
a first resist layer with a first surface coupled to said substrate, said first resist layer having a first resist ~~open~~ developed area;
[[a]] an opaque barrier layer on a second surface of said first resist with a barrier layer ~~open~~ developed area;
a second resist layer coupled to said opaque barrier layer, said second resist layer having a second resist ~~open~~ developed area; and
wherein said first resist ~~open~~ developed area is developed ~~subject to develop~~ subsequent to ~~develop of~~ said second resist ~~open~~ developed area.

2. (Currently amended) The structure of claim 1, further comprising a second opaque barrier layer on said second resist layer with a second barrier layer ~~open~~ developed area, and a third resist layer on said second opaque barrier layer with a third resist ~~open~~ developed area, wherein said second resist ~~open~~ developed area is developed ~~subject to develop~~ subsequent to ~~develop of~~ said third resist ~~open~~ developed area.

3. (Currently amended) The structure of claim 1, wherein said first resist ~~open~~ developed area, said barrier layer ~~open~~ developed area, and said second resist ~~open~~ developed area have variable patterns.

4. (Original) The structure of claim 1, further comprising a plurality of said structures on said substrate.

5. (Currently amended) The structure of claim 1, wherein said first resist ~~open~~ developed area, said barrier layer ~~open~~ developed area, and said second resist ~~open~~ developed area have variable sizes.

6. (Currently amended) The structure of claim 1, wherein said opaque barrier layer is an opaque metallic layer.

7. (Currently amended) The structure of claim 1, wherein said first resist layer and said second resist layer are selected from at least one of the group consisting of: azide, polymers and copolymers of polymethylmethacrylate (PMMA), and resist of SU-8.

8. (Original) The structure of claim 1 wherein said substrate is selected from at least one of the group consisting of: silicon, gallium arsenide, germanium, glass, and metal.

9. (Currently amended) A method of fabricating a multi-layer lithographic semiconductor, comprising:
applying a first resist layer to a semiconductor substrate;
masking said first resist layer and exposing said first resist layer, thereby forming a first latent image in said first resist layer;
adding [[a]] an opaque barrier layer to said first resist layer covering said first latent image;
applying a second resist layer to said opaque barrier layer;
masking said second resist layer and exposing said second resist layer, thereby forming a second latent image in said second resist layer;
removing said second latent image;
etching said opaque barrier layer; and
removing said first latent image.

10. (Original) The method of claim 9, further comprising preparing said substrate.

11. (Original) The method of claim 9, further comprising applying post-application resist treatments.

12. (Original) The method of claim 11, wherein said post-application resist treatments are selected from at least one of the group consisting of: softbake, hydration, and ammonia based image reversal.

13. (Original) The method of claim 9, wherein a shape of said first latent image and the second latent image is selected from the group consisting of: square, rectangle, triangle, circle, oval, and polygon.

14. (Original) The method of claim 9, wherein said etching is selected from the group consisting of wet etch, dry etch and develop/exposure.

15. (Original) The method of claim 9, wherein said exposing uses rays selected from at least one of the group consisting of ultraviolet light, electrons, and x-rays.

16. (Original) The method of claim 9, further comprising using alignment tools.

17. (Currently amended) The method of claim 9, further comprising adding a second opaque barrier layer on said second resist layer, applying a third resist layer on said second opaque barrier layer, masking said third resist layer and exposing said third resist layer, thereby forming a third latent image in said third resist layer, removing said third latent image, etching said second opaque barrier layer, and removing said second latent image.

18. (Currently amended) A lithographic process for fabricating multi-layer semiconductor devices, comprising:
providing a substrate;
coating a first resist layer onto said substrate;
exposing said first resist layer with a mask to form a first layer exposed area and a first layer unexposed area;
depositing [[a]] an opaque barrier layer on said first layer exposed area and said first layer unexposed area;
coating a second resist layer onto said opaque barrier layer;
exposing said second resist layer with a mask to form a second layer exposed area and a second layer unexposed area;
developing said second layer exposed area;
etching said opaque barrier layer;
developing said first layer exposed area; and
fabricating devices on said substrate.

19. (Original) The lithographic process according to claim 18, wherein said depositing is selected from the group consisting of: thermal evaporation, spin coating, spray coating, and electroless plating.

20. (Original) The lithographic process according to claim 18, wherein said step of coating is spun coating.